What is claimed is:

1. A driver circuit comprising:

an output interface;

a pre-drive drive system coupled to a first supply voltage and to a first control signal and a second control signal, and having a fall time control function;

a discharge system, coupled to the pre-drive system at a first node and a second node, coupled to the output interface, and having a switching structure and a discharge structure;

an output structure, coupled to a second supply voltage, to the pre-drive system at the first node, to the discharge system, and to the output interface;

wherein the circuit is adapted to, responsive to assertion of the first control signal, deactivate the discharge system, activate the output structure and supply an output drive signal to the output interface, and, responsive to assertion of the second control signal, activate the discharge system, deactivate the output structure and discharge the output structure, through the output interface, at a rate determined by the fall time control function.

2. The circuit of claim 1, wherein the driver circuit comprises a high side output driver circuit.

3. The circuit of claim 1, wherein the driver circuit is implemented within a semiconductor device.

4. The circuit of claim 3, wherein the output interface comprises a pin on the semiconductor device.

5. The circuit of claim 1, wherein the pre-drive system further comprises:

a first resistive element, having a first terminal coupled to the first node and a second terminal coupled to the second node;

a second resistive element, having first terminal, and a second terminal coupled to ground;

a first transistor, having a first terminal coupled to the first supply voltage, a second terminal coupled to the first control signal, and a third terminal coupled to the first terminal of the first resistive element; and

a second transistor, having a first terminal coupled to the second terminal of the first resistive element, a second terminal coupled to the second control signal, and a third terminal coupled to the first terminal of the second resistive element;

wherein the fall time control function comprises the first and second resistive elements.

6. The circuit of claim 5, wherein the first resistive element comprises a fixed value resistor.

7. The circuit of claim 5, wherein the second resistive element comprises a fixed value resistor.

8. The circuit of claim 5, wherein the first and second transistors are formed of complementary material types.

9. The circuit of claim 5, wherein the first transistor is a P-type MOS transistor and the second transistor is an N-type MOS transistor.

10. The circuit of claim 1, wherein the output structure comprises a transistor, having a first terminal coupled to the second voltage supply, a second terminal coupled to the first node, and a third terminal coupled to the output interface.

11. The circuit of claim 10, wherein the transistor is an N-type MOS transistor.

12. The circuit of claim 1, wherein the discharge system further comprises:

a switching structure, having a first terminal coupled to the first node, a second terminal coupled to the second node, and a third terminal coupled to a third node;

a discharge structure, having first terminal coupled to the first node, a second terminal coupled to the third node, and a third terminal coupled to the output interface; and

a resistive element, having a first terminal coupled to the third node and a second terminal coupled to the output interface.

13. The circuit of claim 12, wherein the discharge structure comprises a transistor.

14. The circuit of claim 12, wherein the discharge structure and the output structure are formed of matching material types.

15. The circuit of claim 14, wherein the discharge structure and the output structure each comprise an N-type MOS transistor.

16. The circuit of claim 12, wherein the switching structure comprises a transistor.

17. The circuit of claim 16, wherein the switching structure and the discharge structure are formed of complementary material types.

18. A method of providing a driver circuitry segment having a particular output signal fall time, the method comprising the steps of:

providing an output interface;

providing a pre-drive drive system, coupled to a first supply voltage and first and second control signals, having a fall time control function;

providing a switchable discharge system, coupled to the pre-drive system at a first node and a second node, coupled to the output interface;

providing an output structure, coupled to a second supply voltage, to the pre-drive system at the first node, to the discharge system, and to the output interface;

operating the pre-drive system, the discharge system and the output structure such that, responsive to assertion of the first control signal, the discharge system is deactivated and the output structure is activated to supply an output drive signal to the output interface, and, responsive to assertion of the second control signal, the discharge system is activated and the output structure is deactivated and discharges, through the output interface, at a rate determined by the fall time control function.

19. The method of claim 18, wherein the step of providing a fall time control function further comprises providing a plurality of resistive elements within the pre-drive system, configured to induce the particular output signal fall time at the output interface.

20. The method of claim 18, wherein the steps of providing an output structure and providing a switchable discharge system further comprise providing, in each structure, a transistor of a matching material type.

21. An output driver circuit formed within a semiconductor device, the circuit comprising:

an output interface;

a first transistor, having a first terminal coupled to a first voltage supply, a second terminal coupled to a first control signal, and a third terminal coupled to a first node;

a first resistive element, having a first terminal coupled the first node, and having a second terminal coupled to a second node;

a second resistive element, having a first terminal, and having a second terminal coupled to ground;

a second transistor, having a first terminal coupled to the second node, a second terminal coupled to a second control signal, and a third terminal coupled to the second terminal of the second resistive element;

a third transistor, having a first terminal coupled to the first node, a second terminal coupled to the second node, and a third terminal coupled to a third node;

a third resistive element, having a first terminal coupled to the third node, and having

a second terminal coupled to the output interface;

a fourth transistor, having a first terminal coupled to the first node, a second terminal coupled to the third node, and a third terminal coupled to the output interface; and

a fifth transistor, having a first terminal coupled to a second voltage supply, a second terminal coupled to the first node, and a third terminal coupled to the output interface.